CLAIMS:

1. A Phase Locked Loop comprising a frequency detector including a balanced quadricorrelator, the loop being characterized in that the quadricorrelator comprises double edge clocked bi-stable circuits coupled to multiplexers being controlled by a signal having the same bitrate as the incoming signal.

2. A Phase Locked Loop as claimed in claim 1, wherein a first pair of double edge clocked bi-stable coupled to a first multiplexer and a second pair of double edge clocked bi-stable coupled to a second multiplexer are supplied by mutually quadrature phase shifted signals respectively to provide a first signal and a second signal indicative for a phase difference between the incoming signal and mutually quadrature phase shifted signals.

3. A Phase Locked Loop as claimed in claim 2, wherein the mutually quadrature phase shifted signals are generated by a voltage controlled oscillator.

4. A Phase Locked Loop as claimed in 2, wherein a third pair of double edge clock bi-stable coupled to a third multiplexer and a fourth pair of double edge clock bi-stable coupled to a fourth multiplexer are supplied by the first signal and the second signal, respectively.

5. A Phase Locked Loop as claimed in claim 4, wherein the quadricorrelator further comprises a first adder for adding a third signal provided by the third multiplexer to a fourth signal provided by a fourth multiplexer and generating an error signal indicative for a frequency difference between the incoming signal and mutually quadrature signals.

6. A Phase Locked Loop as claimed in 5, wherein the error signal is inputted to a coarse control input of the voltage controlled oscillator via a first charge pump coupled to a first low-pass filter coupled to a second adder.

7. A Phase Locked Loop as claimed in claim 6, wherein a fine control input is controlled by a signal provided by a phase detector coupled to a second charge pump coupled to second low-pass filter.